EDA TOOLBOX FOR VHF DATA LINK SYSTEM SIMULATION

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SUMMARY

In today's commercial air traffic, communication via digital data links has become vital to cope with the increase in traffic density. VHF Data Link Mode 2 (VDLm2) is currently in use for controller pilot digital link communications (CPDLC). VFH Data Link Mode 4 (VDLm4) is currently under evaluation as a candidate technology for Automatic Dependent Surveillance (ADS-B), multilateration, and point-to-point data transmission. Electronic design automation software is widely in use for engineering of communication systems. For commercial transmission systems like GSM or UMTS libraries and toolboxes are available within the software allowing for short development cycles. In aviation, due to the smaller market for EDA tools, this is not valid: low-level functional blocks are to be adopted for this specific purpose and used instead.

To improve this situation a library for use with commercially available EDA software (Advanced Design System, Agilent Technologies) consisting of functional blocks was developed. The library enables radio frequency (RF) development engineers to perform system level simulations – using specialised simulation components dedicated to VHF Data Link (VDL) simulation. As the scope of the EDA software used is in the RF front-end and digital signal processing (DSP) domain, functional blocks within the physical layer of VDL were defined. For both VDLm2 and VDLm4 system components replacing basic digital RFIC functionality were made available. On the transmit side they convert a raw data bit stream into channel coded signals which are further transformed into I/Q data modulating a user-selectable carrier frequency. On the receive side demodulation and decoding to recover the original bit stream were implemented. Other functionalities like power ramp up/down are available. VDL specific modulation schemes (D8PSK in VDLm2, GFSK in VDLm4) are used in these components. The sub-blocks used were also made available as stand-alone functional elements to provide flexibility, e.g. to allow engineers using their own base band formulation programmed in MATLAB by running co-simulation. The library was tested and verified using a VDLm2 system simulation set-up as well as a VDLm4 signal generation application. Signal compliance to standards was tested using the I/Q output of the library components created as a source for vector signal generation with quadrature modulation input.

The toolbox presented in this paper is intended to speed-up development cycles by providing ready-to-use VDL functional blocks to RF system engineers. It provides VDL-compliant components for development of transmitters and receivers used in communications equipment. It is also a powerful tool to be used in teaching of students focussing to CNS technologies.

1. INTRODUCTION

While air traffic growths steadily since several years a gap in communication capacities – both voice and data – rose. To close this gap new digital communication standards were standardized by ICAO [1]. Future ATC concepts like EUROCONTROLS LINK2000+ programme [2] take advantage of such links as they are key technologies to overcome capacity bottlenecks due to both increase in air traffic and shortage in frequency.

Today several electronic design automation tools are available which provide powerful capabilities for RF system design, electromagnetic simulation/verification of RFIC or board layout, as well as digital signal processing (DSP). They are shipped with libraries comprising popular communications standards like GSM, 3GPP, DVB and others. Due to the smaller market segment aerospace related libraries are rare. Also proprietary or emerging standards are not covered.

To enhance both development of aeronautical communication systems and education on university in the field of ATC technologies a library for RF system simulation of aeronautical communication standards was generated.

2. METHODS

To develop the aeronautical system library an integrated simulation environment was used. The specifications for the physical layer of the communication standards were summarized, mathematically formulated, implemented, and made available in the design tool chosen. Verification was carried out to ensure compliance with the standards.

2.1. Simulation Environment

The work was carried out using Advanced Design System (ADS, Agilent Technologies), which is an industry-standard commercial EDA software tool for RF system, IC, and circuit engineering. It provides different simulators, of which Ptolemy simulation, a synchronous data flow technique developed by University of California in Berkeley was used here [3]. The software also provides interfaces towards signal generators and analyzers. Using this feature simulated signals can be used to form real-world signals, e.g. for verification of hardware systems and

components [4, 5]. The complete simulation environment (including link to test equipment) is shown in FIG 1.

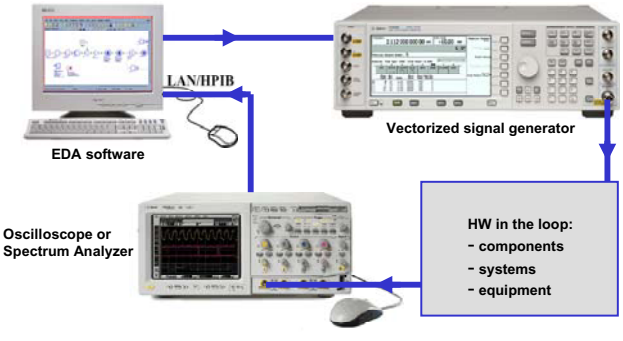

FIG 1. Overview of the simulation environment [4, 5].

2.2. VHF Data Link

To cope with the prognosted further increase in air traffic the International Civil Aviation Organization (ICAO) has standardised a concept for an Aeronautical Telecommunications Network (ATN) which integrates ground, air-to-ground, and avionics data segments into an interoperable system (FIG 2) [1].

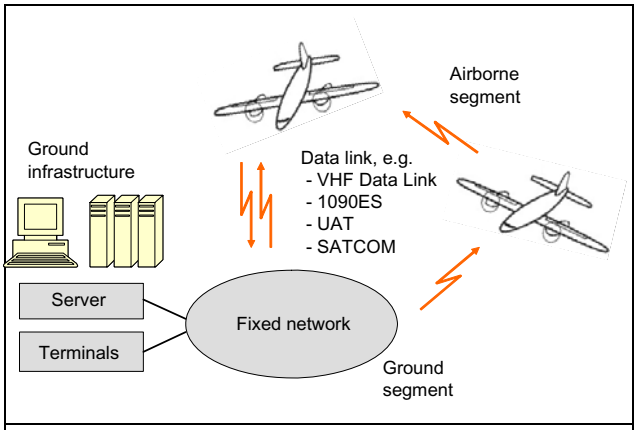

FIG 2. Concept of the Aeronautical Telecommunications Network (ATN).

The air-to-ground interface is formed by HF data link (HFDL), VHF data link (VDL), SSR Mode S (1090ES), and aeronautical Satellite communications (i.e. AMSS-1) to support applications as Automatic Dependent Surveillance (ADS-B), Controller-Pilot Data Link Communications (CPDLC), ATIS, or routine weather report services (METAR) [1].

2.2.1. VDL Physical Layer Summary

VDL itself is sub-divided into different modes, of which Mode 2 (VDLm2) and VDL Mode 4 (VDLm4) are further discussed here. They differ in the way how they access the communication channel (i.e. modulation scheme, signal shaping filter), in the transmission capacity provides to the application, and in the timing requirements of the transmission path. A comparison of the parameters of the physical layer for both modes is given in TAB 1. The timing diagrams of a transmission protocol for VDLm2 and VDLm4 are presented in FIG 3 and FIG 4. Both systems have in common that the power-up phase is followed by a training sequence to allow the receiver to get synchronised with the transmission. While output power in VDLm4 has to be established at a minimum of 90% of the manufacturer's declared output power when the training sequence begins, the ramp-up phase in VDLm2 has to be finished 2.5 symbol times prior to the first symbol in the synchronisation phase (measured from the nominal start time of the transmission at 50% of the first symbol's time slot).

This requires implementing a power ramp controller as an element of the EDA toolbox for proper simulation of the physical layer behaviour. Control of the power ramp function is carried out by a transmit/receive signal which would be provided by a baseband processor (not covered in this work).

2.2.2. VDLm2 Implementation

The implementation of VDLm2 specifications was divided into three components responsible for D8PSK modulation, D8PSK demodulation, and power ramp control. These elements were integrated to form a system-level representation of a digital RFIC providing VDLm2 compliant transceiver functionality.

The modulator includes conversion from bits to symbols, Gray coding, differential phase shift keying, and Raised Cosine filtering. Symbols are formed by combining 3 consecutive bits of the binary data stream into a symbol (octet). By this the VDLm2-specific bit rate is converted into a symbol rate of *10 500 baud*:

$$(1)\quad s[k] = b_{0,LSB}[n-2]\cdot 2^0 + b_1[n-1]\cdot 2^1 + b_{2,MSB}[n]\cdot 2^2$$

In the second data processing step both Gray coding and calculation of the 8 phase shifts related to the octets to be transmitted are performed:

$$(2)\quad \Delta\phi[k] = \frac{\pi}{4}\begin{cases}0\\1\\3\\2\\6\\7\\5\\4\end{cases};\quad s[k] = \begin{cases}0\\1\\2\\3\\4\\5\\6\\7\end{cases}$$

The parameter ϕ is modulating the carrier frequency ω_c in the transmitter. The modulated waveform is represented as a complex symbol, using I and Q as in-phase (real) and quadrature (imaginary) components of the complex symbol:

$$(3)\quad \underline{U}(t) = A\,e^{j(\omega_c t+\phi[k])} = A\left(I[k] + j\,Q[k]\right)e^{j(\omega_c t)}$$

As VDLm2 transmits the input data in differential form, phase changes due to the input has to be calculated. The

Parameter	VDL Mode 2 [1, 6]	VDL Mode 4 [1, 7, 8, 9]
Bit rate	$f_{bit} = 31\ 5200\ 1/s = 1/T_{bit}$	$f_{bit} = 19\ 200\ 1/s = 1/T_{bit}$
Timing	Symbol rate: 125 $f_{Symbol} = 10\ 500\ 1/s = 1/3\ f_{bit}$	1 super frame ($60\ s$) = 4500 slots 1 time slot ($13.333\ ms$) = 256 bit
Coding of binary data	$\{b_{0,LSB}[n-2]\ b_1[n-1]\ b_{2,MSB}[n]\} \rightarrow \{s[k]\}$; Gray coding	NRZ-I: starting with "high" tone in the training sequence, toggling when transmitting "zero" bit
Modulation scheme Pulse shape filter	D8PSK Raised Cosine filter, $\alpha = 0.6$	GFSK, $m = 0.25 \pm 0.03$ ($=2\Delta f/T_{bit}$) Gaussian filter, $BT = 0.28 \pm 0.03$ ($=B \cdot T_{bit}$)
Carrier frequency range Bandwidth	$118.000\ (108.000) - 136.975\ MHz$ $25\ kHz$ bandwidth	$118.000\ (108.000) - 136.975\ MHz$ $25\ kHz$ bandwidth
MAC	Carrier Sense Multiple Access (CSMA)	Self-organizing TDMA (STDMA)
Signal-to-Noise ratio		$SNR = 10\ dB$
Synchronisation		UTC time (e.g. using GNSS)

TAB 1. Summary of VDLm2 and VDLm4 physical layer key parameters.

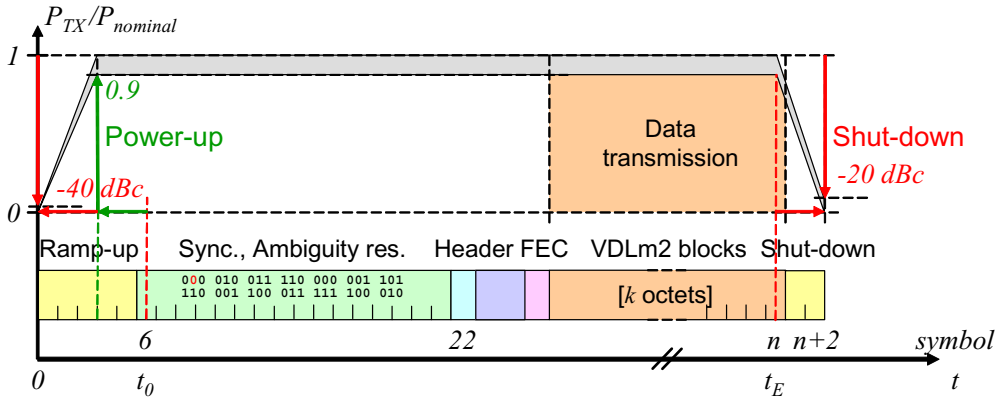

FIG 3. Timing diagram of a VDLm2 transmission, consisting of ramp-up phase, synchronisation and ambiguity resolution phase, header, forward error correction (FEC) data, data transmission phase, and shut-down phase.

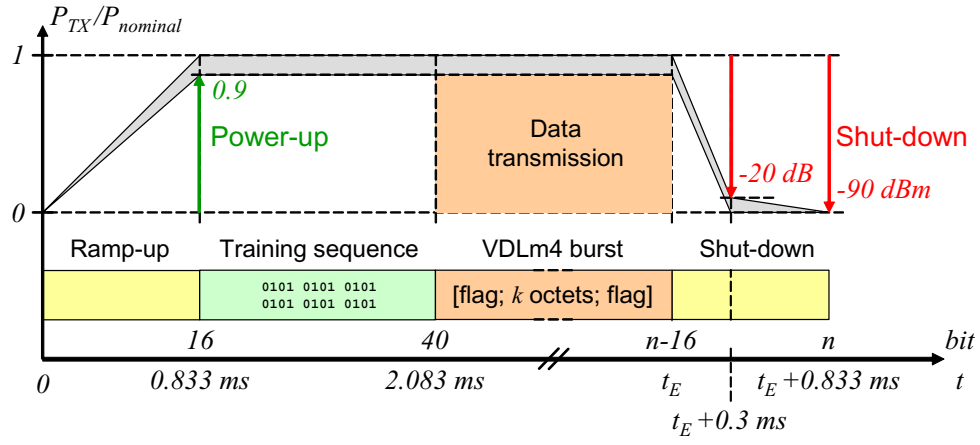

FIG 4. Timing diagram of a VDLm4 transmission, consisting of ramp-up phase, training (synchronisation) phase, VDLm4 burst (data and start/stop flag), and shut-down phase.

I/Q pair is derived from its predecessor with aims of geometrical considerations (FIG 5):

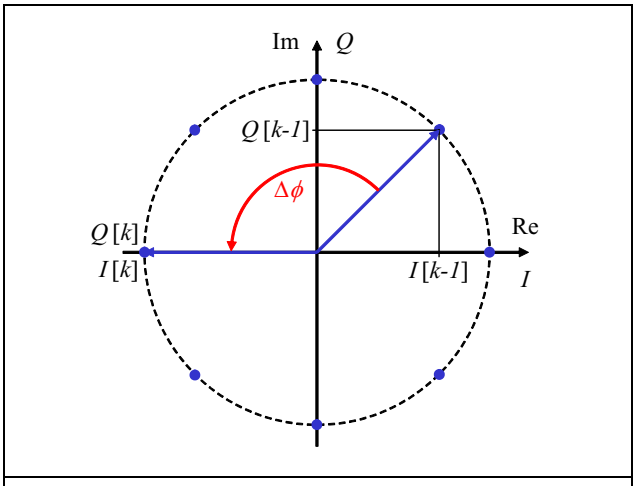

FIG 5. Representation of phase shifts in the *I/Q* constellation diagram.

Using trigonometrically expressions the relations necessary can be formulated:

$$(4)\quad \begin{aligned} I[k] &= \cos(\Delta\phi)I[k-1] - \sin(\Delta\phi)Q[k-1] \\ Q[k] &= \sin(\Delta\phi)I[k-1] + \cos(\Delta\phi)Q[k-1] \end{aligned}$$

To fit into the *25 kHz* spacing of the communication channels, excessive bandwidth consumption is reduced using Raised Cosine (RC) filters for pulse shaping on both channels. The frequency response $f(\omega)$ of a RC filter is *1* (*0*) below (above) the cut-off frequency ω_c minus (plus) α percent of ω_c (called roll-off factor). The transition of the frequency response follows a raised cosine function (e.g. [10]):

$$(5)\quad \begin{aligned} F(\omega) &= \ldots \\ \ldots &= \begin{cases} 1; & \omega < \omega_c(1-\alpha) \\ \frac{1}{2}\left(1+\cos\frac{\pi(\omega-\omega_c(1-\alpha))}{2\alpha\omega_c}\right); & \omega_c(1-\alpha) \le \omega < \omega_c(1+\alpha) \\ 0; & \omega \ge \omega_c(1+\alpha) \end{cases} \end{aligned}$$

The resulting signals $U_I(t)$ and $U_Q(t)$ are then used to modulate the carrier using a quadrature amplitude modulator (QAM). Its output power is set to *0 dBm* using a constant *k*, the carrier frequency ω_c is user-definable:

$$(6)\quad \underline{U}_{VDLm2}(t) = k \cdot \left(U_I(t) + jU_Q(t)\right) \cdot e^{j\omega_c t}$$

On the receive path these steps are performed in a converted order. First the demodulation of the receive signal is carried out. Using a QAM demodulator the signals $U_I(t)$ and $U_Q(t)$ were made available. By sampling $U_I(t)$ and $U_Q(t)$ in the middle of a time slot $I[k]$ and $Q[k]$ are generated. Input power of the demodulator is recommended to be *0 dBm* using appropriate amplification.

To overcome changes in the magnitude, the signal vector length a is calculated to normalize *I/Q*:

$$(7)\quad I[k] = \frac{I'[k]}{\sqrt{I'[k]^2 + Q'[k]^2}}; \quad Q[k] = \frac{Q'[k]}{\sqrt{I'[k]^2 + Q'[k]^2}}$$

Having $I[k]$ and $Q[k]$ available the phase angles $\phi[k]$ are known, $\Delta\phi$ is calculated by considering the difference between two neighboured phase angles:

$$(8)\quad \Delta\phi = \phi[k] - \phi[k-1]$$

By this the complexity of D8PSK demodulation is reduced to 8PSK demodulation. In the final step the phase difference is attributed to the symbol $s[k]$ (represented by a triplet of bits). Gray code is converted back to BCD. To facilitate bit error rate (BER) calculations, the order of the least and most significant bit is converted to match the order of input binary stream:

$$s[k] = b_{0,LSB}[n-2]\cdot 2^0 + b_1[n-1]\cdot 2^1 + b_{2,MSB}[n]\cdot 2 = \ldots$$

$$(9)\quad \ldots = \frac{4}{\pi}\Delta\phi \begin{cases} 0 \\ 4 \\ 6 \\ 2 \\ 7 \\ 3 \\ 1 \\ 5 \end{cases}; \quad \Delta\phi = \frac{\pi}{4} \begin{cases} 0 \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \end{cases}$$

For the power ramp function the transmit/receive signal provided by the baseband component is used to define control signals of an 8-bit counter which is used to generate a ramp. The original TX/RX signal defines weather the counting direction is up or down. An “Enable” signal allows the counter to run in either direction (defined by TX/RX state) as long as the current state of the counter is between its minimum and maximum. The ramp is used as input signal for a cosine function generating a smooth transition between minimum output power and maximum output power:

$$(10)\quad \begin{aligned} Up/\overline{Down} &= TX/\overline{RX} \\ Enable &= \left(\overline{TX/\overline{RX}} \wedge \overline{Ctr=0}\right) \vee \left(TX/\overline{RX} \wedge \overline{Ctr=208}\right) \\ Ramp[k] &= -\frac{1}{2}\left(\cos\left(\frac{Ctr[k]}{208}\pi\right)+1\right) \end{aligned}$$

As an example for the implementation of the mathematical description of the components into the EDA environment the circuit of the power ramp logic is presented in FIG 6.

The three functional blocks described above were combined into a common component emulating a VDLm2 RFIC with direct generation of the RF output signal.

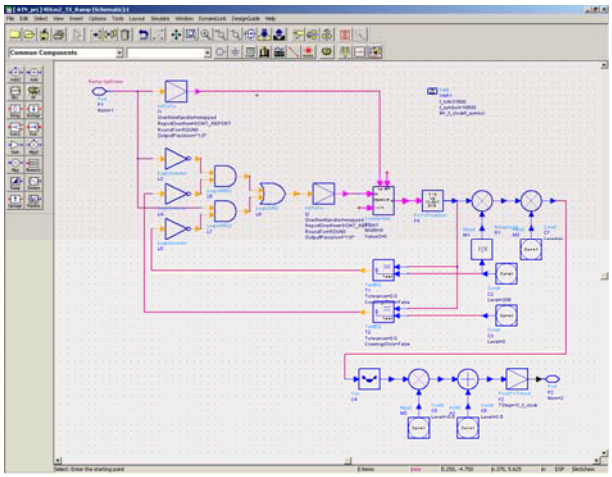

FIG 6. Implementation of the power ramp logic in the EDA environment. A counter (centre) is controlled by combinatory logic elements. The output generates the slope of the power ramp signal.

2.2.3. VDLm4 Implementation

For VDLm4 the same steps as for VDLm2 were performed: components responsible for GFSK modulation, GFSK demodulation, and power ramp control were mathematically described and implemented using functional blocks of the EDA tool. These elements were integrated to form a system-level representation of a digital RFIC providing VDLm4 compliant transceiver functionality.

In VDLm4 the binary input data stream is NRZ-I coded. According to the relevant standards [1, 7, 8, 9] the logical state of the coder's output is toggled when logical "zero" is to be transmitted:

$$(11)\quad b'[n] = \begin{cases} \bar{b}[n-1]; & b[n]=0 \\ b[n-1]; & b[n]=1 \end{cases}$$

Using the NRZ-I line code logical states are converted into physical levels of voltage:

$$(12)\quad u[n] = \begin{cases} -1V; & b'[n]=0 \\ +1V; & b'[n]=1 \end{cases}$$

Similar to VDLm2 a pulse shaping filter is used to reduce bandwidth consumption of the transmit signal. Here, Gaussian filtering with a product BT equals filter bandwidth times symbol period of 0.28 is implemented. The frequency response of the Gaussian filter can be derived from using Laplace transformation of its Gaussian shaped impulse response $h(t)$ [11]:

$$(13)\quad F(\omega) = H(s)\big|_{s=j\omega} \quad \bullet\!-\!\circ \quad h(t) = \frac{e^{\frac{-t^2}{2\delta^2}}}{\sqrt{2\pi}\cdot\delta}; \quad \delta = \frac{\sqrt{\ln(2)}}{2\pi\cdot BT}$$

The resulting signal is used as input for a conventional frequency modulator:

$$(14)\quad \underline{U}_{VDLm4}(t) = k\, e^{j\left(2\pi\int_0^t (f_c+\Delta f\, u(t))dt\right)}$$

Again, output power of the modulator is set to $0\ dBm$ using a constant k, the carrier frequency ω_c is user-definable.

After demodulation of the FM signal a limiter is used to detect zero-crossings of the signal and to recover the NRZ-I coded signal. The bipolar signal's level is converted into logical stages and used to get the original bit stream out of the NRZ-I coded signal:

$$(15)\quad b[n] = \left(b'[n] \oplus b'[n-1]\right); \quad b'[n] = \begin{cases} 0; & u[n]=-1V \\ 1; & u[n]=+1V \end{cases}$$

The power ramp element is using the same architecture as with VDLm2. To account for the higher bit rate a different clock frequency was used here to control the internal counter.

2.3. Verification of the Toolbox: Case Studies

Verification of the elements provided in the toolbox was carried out using two case studies, one for each VDL mode. The VDLm2 RFIC element was tested in a set-up for a system simulation of a communication transceiver. For this a two-stage PA was used. The first PA's power gain was controlled by the RFIC using the power ramp line. The second PA was using a fixed gain. The channel was modelled using an ideal matched loss element. On the receive chain a conventional single down-conversion receiver element was used. Results were also compared with an alternative D8PSK approach involving a MATLAB co-simulation [11]. The set-up of the simulation is displayed in FIG 7.

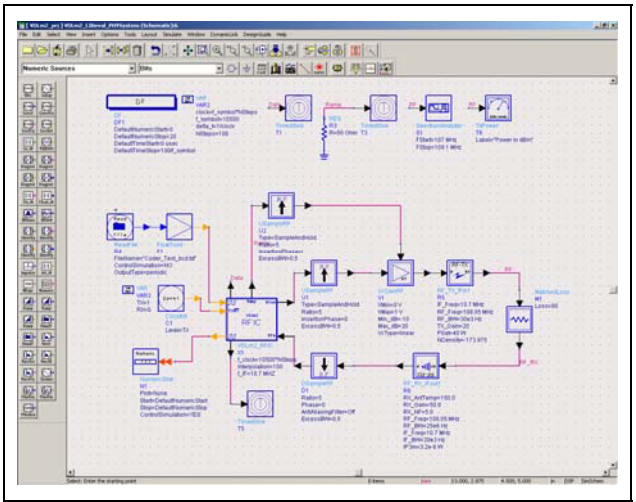

FIG 7. Set-up of the VDLm2 physical layer simulation using the EDA toolbox.

For VDLm4 the signal provided by the RFIC element was used to feed a vectorized signal generator (E4432B, Agilent Technologies) with arbitrary I/Q function via USB/GPIB interface. With different types of pre-defined

bursts real-world signals were generated and compared to the simulation [5, 12]. The test set-up used is shown in FIG 8.

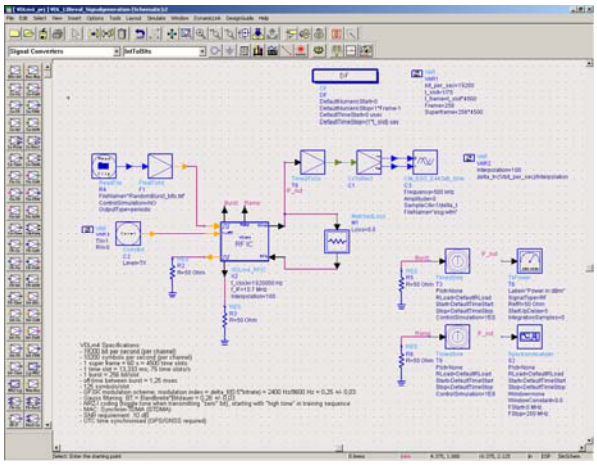

FIG 8. Set-up of the VDLm4 signal generation using the EDA toolbox.

Three tests signals were generated and compared with the simulated signal: (a) a burst producing a low tone response in the modulator, (b) a burst corresponding to an alternating bit stream as input to the modulator, and (c) a valid random burst. All of them included a VDLm4 preamble. Measurement of the signals was made using a deep memory scope with large bandwidth (54832D, Agilent Technologies).

3. RESULTS

In the following section the resulting VDL library as well as the findings of the case studies is shown.

3.1. VDL Library

Each function described mathematically is placed in a "VDL System Library". This library is available in the EDA environment for use with other designs (FIG 9).

Each of the two VDL modes covered is supported by specific modulation, demodulation, power ramp, and RFIC components. Key parameters are user definable (FIG 10).

3.2. Case Study 1: VDLm2 System Simulation

In FIG 11 the dynamic range of the transmitter is shown. The blue power spectrum is taken for a nominal transmit state of the transceiver ($P_{out} = 40\ dBm$). With the power amplifiers (PA) turned on and the RFIC is in receive mode, the red power spectrum is measured ($P_{out} = 0\ dBm$). The difference corresponds to the dynamic range of $40\ dB$ related to the power ramp function of the RFIC.

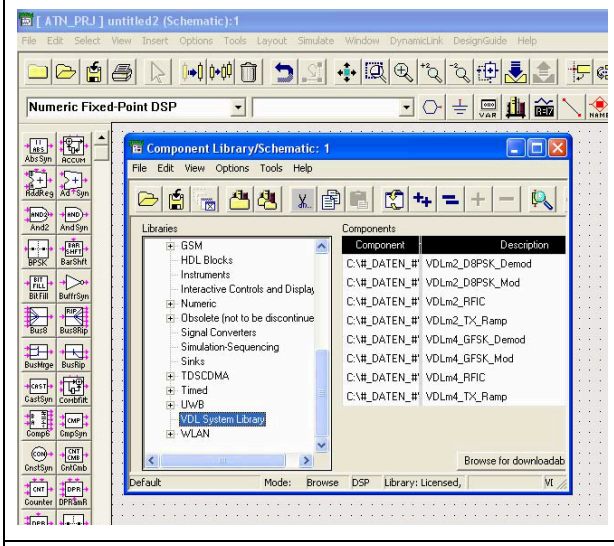

FIG 9. VDL system library implemented in the EDA environment.

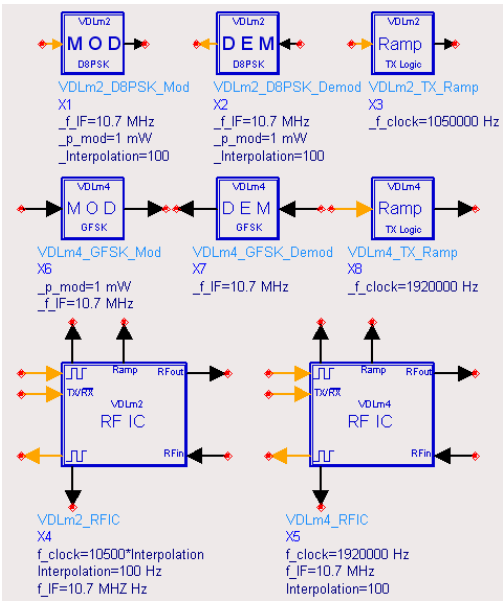

FIG 10. Elements created in in the VDL system library (from above: VDLm2 modulation, demodulation, power ramp, RFIC, VDLm4 modulation, demodulation, power ramp, and RFIC).

The I/Q constellation diagram of the transmitted signal generated by the VDLm2 RFIC is displayed in FIG 12. For this the binary input consists of a random generator. This results in a constellation diagram showing the 8 states of the D8PSK modulation and all possible paths between them. Curving of the connections is due to the pulse shaping filters.

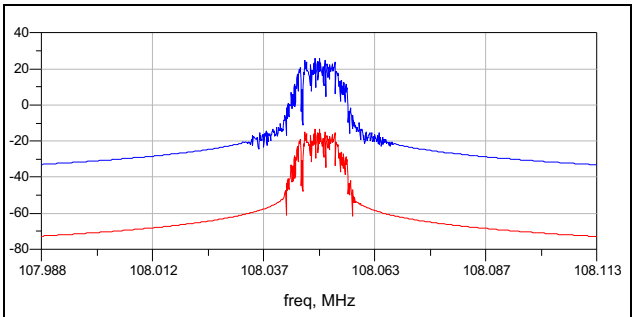

FIG 11. RF spectrum of random bit stream at antenna port. Blue: RFIC switched in TX mode. Red: RFIC in RX mode, PA powered-up (RX-to-TX turn-over).

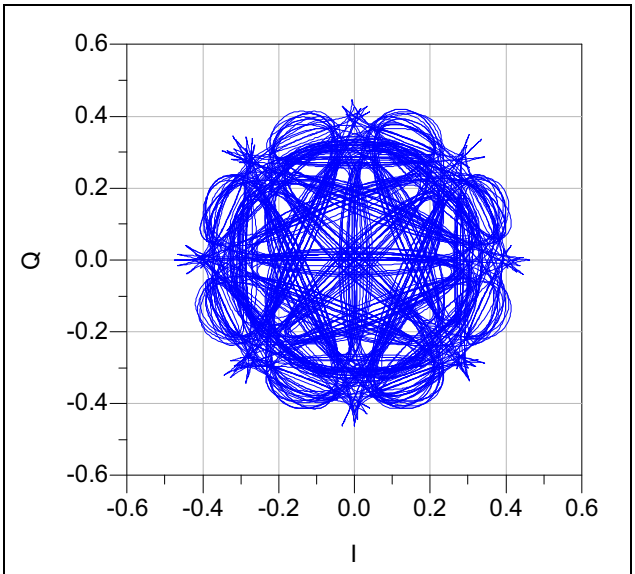

FIG 12. I/Q constellation diagram of the transmit RFIC signal.

3.3. Case Study 2: VDLm4 Signal Generation

In this study the VDL library is used to generate a VDLm4 test signal, e.g. for receiver or component testing (as with [5, 12]). FIG 13 shows the spectrum due to a VDLm4 burst generating a permanent “low tone”, corresponding to a *-2.4 kHz* frequency deviation from the carrier frequency. The simulated (grey colour) and the generated signal (amber colour) correspond well.

An alternating logical “zero”/logical “one” bit series as the modulator’s input signal produces a spectrum where the maximum signal frequency of half the specified VDLm4 bit rate (*9,6 kHz*) can be seen in the spectrum. Again, measurement of the generated signal (amber) and simulation (grey) are in good accordance (FIG 14).

Also using a random test burst (including a real-world VDLm4 header with synchronization phase, flag, random data, and flag) for signal generation, well agreement between simulated signal and measurement can be seen (FIG 15).

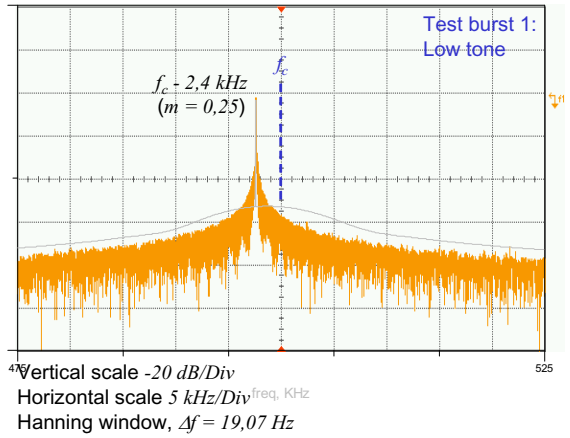

FIG 13. Comparison between simulated (grey) and measured (amber) signal for test burst 1.

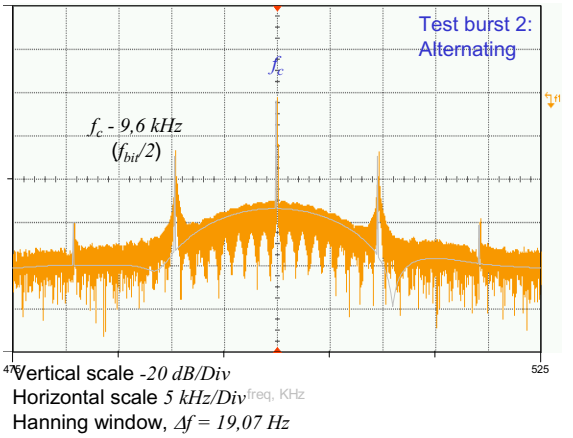

FIG 14. Comparison between simulated (grey) and measured (amber) signal for test burst 2.

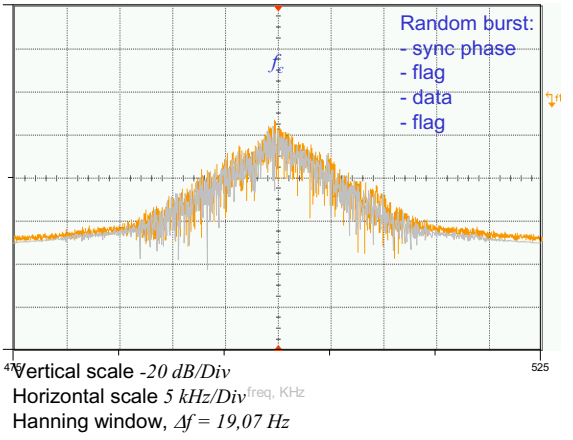

FIG 15. Comparison between simulated (grey) and measured (amber) signal for a VDLm4 random burst.

4. DISCUSSION

With the EDA toolbox generated a powerful tool is available to perform for example link budget simulations, signal generation, or demonstration of system behaviour in lecture courses. Key features of VDL were implemented in a ready-to-use library in the EDA environment. Possible applications in physical layer system simulation and test signal generation were demonstrated.

The RFIC functionality was kept rather basic. In future work more enhanced power control technologies could be implemented. This could be done by using fast closed-loop architectures. On the receive side neither power sensing nor LNA gain control mechanisms are implemented. This would also be a possible area for improvements.

On the demodulation functions rather straight forward approaches were taken. By applying more sophisticated routines better robustness against noise and therefore improvements in bit error rate respective frame (symbol) error rate could be achieved.

A further aspect for improvement would be in defining digital baseband blocks. They would could include error correction or automated generation of the bursts.

As one main goal of the development was to provide an aeronautical telecommunication systems library, further effort will be spent into design of components dedicated for Mode S data link (and Mode S surveillance RADAR) and satellite communications.

By this further improvement in the development of powerful ATN equipment in terms of air-to-ground interfaces shall be enabled.

5. REFERENCES

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